Adiabatic Logic Based Energy Efficient Architecture of 1-Bit Magnitude Comparator for IoT Applications

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Abstract

The Internet of Things (IoT) applies the sensors and microcontrollers and links them through the internet. The eventual objective of low-power devices for Internet of Things is to lesser the overall system power and to extend battery life. For the development of energy efficient IoT devices, novel adiabatic techniques are proposed. By improving the performance of the comparator, one can improvise the whole system performance. The efficacy of computing devices depends on the performance of arithmetic circuits, including comparator. This paper proposes 1-bit comparator design using adiabatic techniques such as DC-DB PFAL (Direct current diode-based positive feedback adiabatic logic) and MPFAL (Modify positive feedback adiabatic logic) which are well-suited with an extensive range of applications (e.g. IoT sensors and an inbuilt analog to digital converter). For performance analysis, the results are compared together along with the other adiabatic and non adiabatic designs already reported in the literature. This paper proposes a way to decrease the dissipation of power and transistor count in binary circuits as it is one of the primary concerns. From the results, it is found that the design using DC-DB PFAL logic shows an improvement in power-delay-product of 69%, 94% and 90% compared to MPFAL, PFAL and ECRL techniques respectively.

Keywords: Comparator, Adiabatic logic, IoT, Energy efficient

1 Introduction

Our world will be transformed by the Internet of Things. Sensors and cloud computing promise to connect all the "things" that affect our daily lives, paving the way for the next industrial revolution. The community has lot of interest in IoT since it connects and controls machines, devices, and equipment over a network. In today's environment, IoT technology has enabled a variety of devices to communicate and accurately provide data. Many sensors are necessary for the system when using the Internet of Things to collect data or information like humidity, strain, motion, temperature, and magnetic field strength [1]. Now-a-days, the demand for wireless sensors has increased dramatically for the applications of IoT [2]. Its applications include healthcare, industrial sensing, environmental measurements and smart homes [3]. IoT devices require ultra-low power methodologies since they are either heterogeneous battery or energy harvesting. Now-a-days, the number of battery-powered devices is increasing. So, there is a need of low power consumption that enables low power elements to communicate with other components in wireless mode [4]. The requirement of low energy and voltage devices is of prime concern in the present scenario [5].

The Complementary metal-Oxide-Semiconductor technology is common for large scale integration and low dissipation of power [6]. A novel CMOS logic for low power, which is based on the adiabatic switching principle, is called adiabatic logic.

The adiabatic circuit, which reprocesses the charge of node capacitances using AC power supplies, is a way to minimize power dissipation (PD). The term adiabatic is derived from thermodynamics, which means there are no heat losses [7-9]. Adiabatic logic is a promising approach for minimum energy digital circuits that has been proposed recently. Another benefit of the adiabatic logic circuits is that it reduces the switching noise of digital circuits. Over the past decades, the need of ultra-low-power nano-electronics has motivated researchers to come across newer energy improvement strategies in the application of IoT. The magnitude comparator is the essential component of combinational logic circuits and is generally used in low power and low voltage applications, like communication and device processing, ADC converter, and many more.

ADC or DAC converters play a vital role in ICs. The comparator is a crucial component of ADCs and consumes a lot of power in the device. Our main objective is to develop a low-power, high-speed comparator [10-11]. Panda *et al.* suggested an innovative lower power 64-bit CMOS binary comparator. To get a better power delay product (PDP) of the recommended design, changes are made to the conventional 64-bits digital comparator design [12]. In [13], a low power 2-bit magnitude comparator is presented through adiabatic logic and demonstrated an improvement in PDP as compared to the existing traditional designs. Further, by using effective load recovery logic, a 4-bit comparator circuit was designed and demonstrated that the PFAL is more power-efficient as compared to ECRL [14]. In [15], a comparator reported using ECRL and PFAL techniques. It was demonstrated that PFAL technique had shown better performance compared to ECRL technique. Further, the BCL (bitwise competitive logic) based

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high-performance digital comparator was reported [16]. By using full adder technology, a low-power 2-bit magnitude comparator was presented [17]. This introduced a magnitude comparator using Pass Transistor logic as opposed to the magnitude comparator with GDI technique. In addition to this, the implementation of inverter-based low power adiabatic dynamic comparator has been proposed [18], where, back-to-back inverter of a conventional dynamic comparator is being replaced by the Diode free adiabatic logic inverter that utilizes the adiabatic logic concept for power optimization. Various magnitude comparator designs have been reported in the literature [19-21]. Kaza *et al*. has designed secured MPFAL logic for IoT applications. The FinFET technology is used to design an 8-bit replacement box with an energy recovery modified PFAL adiabatic logic [22]. Kumar *et al.* presented a design of an energy-efficient and secure PUF for IoT devices based on adiabatic logic. The proposed adiabatic PUF uses an energy recovery approach to achieve great energy efficiency, as well as a time ramp voltage to provide reliable start-up behavior [23].

Nevertheless, the construction of energy-efficient circuits is a fundamental challenge in low-power VLSI design. In most digital and analog circuits, comparators are widely used as a part of sensor networks, analog to digital converters etc. Thus, it will be beneficial to have high-performance comparators which can improve overall system performance. From the literature survey, it has been observed that the power dissipation of all the non adiabatic and adiabatic comparators reported in the literature needs to be minimized further.

In this paper, using MPFAL and DC-DB PFAL adiabatic logic-based one-bit magnitude comparator circuits is proposed. Further, for performance comparison the 1-bit magnitude comparator is also being proposed using two other adiabatic approaches such as ECRL and PFAL. The results of all the proposed designs have been compared with the other adiabatic and non-adiabatic circuits reported in the literature. It is noteworthy to mention that the comparator circuits using MPFAL and DC-DB PFAL techniques are the first time reported here and have shown improved performance over the rest of the adiabatic methods.

This paper is structured into five sections. Section 2 outlines the fundamentals of adiabatic logic. Section 3 includes the proposed design of magnitude comparator using adiabatic techniques. In Section 4, the results and discussion are described. The paper concludes with section 5.

2 Adiabatic Logic Circuit

An adiabatic circuit is low-power hardware that saves energy using reversible logic [24-25]. The term adiabatic originates from a Greek word that describes thermodynamic procedures which means there is no energy interaction with the environment and as a result, there is no power loss in the form of heat dissipation. In adiabatic logic, a power clock is used instead of using a dedicated power supply for the clock.

Within this, the core design improvements are based on the power clock that acts a crucial task throughout the theory of operation. The adiabatic circuit includes three rules for energy utilization.

1. When there is a large voltage difference between its sources and drain terminals, the transistor must be off.
2. When current is flowing through the transistor, it must be turned on.
3. Never transmit current via a diode.

3 Design of Magnitude Comparator using Adiabatic Techniques

A comparator is a type of combinational logic circuit that compares two inputs and produces outputs which show one is small or greater or an equal in magnitude. Figure 1 depicts the basic 1-bit comparator. It is useful in control applications where the binary integers representing the monitored physical element are compared to the reference values [26-27].

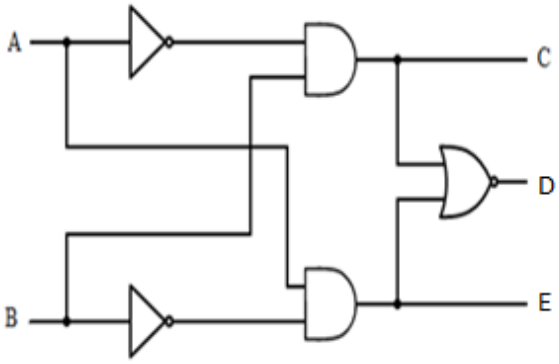

Figure 1. 1-bit comparator block diagram

In Figure 1, let a 1-bit comparator with A and B inputs, where, C= (B>A), E = (A>B) and D = (A=B) are the outputs. If this condition is true then respective output variable logical values are set and vice versa.

3.1 Design of Magnitude Comparator using Efficient Charge Recovery Logic Technique

This section presents the circuit design and simulation of a 1-bit magnitude comparator at 6MHz clock frequency and 180nm technology node. ECRL is amid the mostly used adiabatic methods. This design comprises two M3 with M4 cross-coupled PMOS transistors along with 2- NMOS transistors attached in parallel to N functionally blocks realization for ECRL adiabatic logic. Only NMOS transistors are used for the realization of usable blocks. A power clock supply is used for ECRL gates so that energy can be retrieved and used again. Because the future phases should determine the logical values during the idle stage while the previous stage is in the hold. Figure 2 shows the proposed magnitude comparator design using ECRL technique.

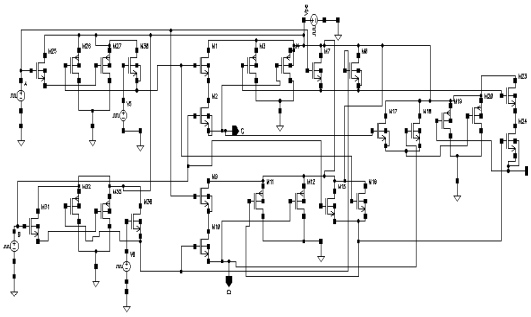

Figure 2. ECRL based comparator

The simulations are run and the outputs are generated. It is analyzed that ECRL based comparator design shows a power dissipation of 23.29 μW, delay of 67.87ns, power delay product of 1.58 pJ, the rise time of 0.974ns, and fall time of 13.52ns at 1.8V.

3.2 Design of Magnitude Comparator using Positive Feedback Adiabatic Logic

Positive feedback adiabatic logic is a recent approach that employs positive feedback cross-coupled inverters to form this logical configuration. NMOS devices connected parallel with PMOS devices decide the logic function in PFAL, exactly as they do in ECRL. In PFAL, the power source is Vpc and it is known as the power clocks, splits into 4- phases. PFAL remains a double-rail circuit that takes complementary inputs and provides complementary outputs. Figure 3 depicts the basic scheme of the PFAL comparator. Power dissipation of 22.54 μW, delay of 67.3 ns, power delay product of 1.516 pJ, the rise time of 9.024 ns, and fall time of 51.06 ns at 1.8V are obtained for the proposed PFAL based 1-bit magnitude comparator circuit which indicates its performance.

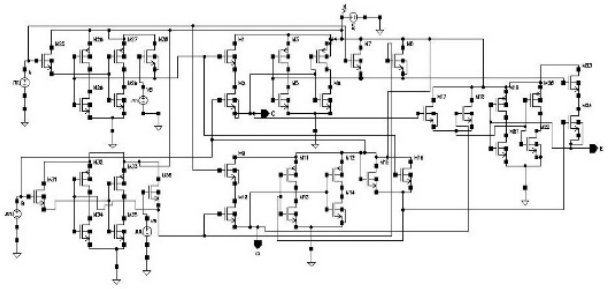

Figure 3. PFAL based Comparator

3.3 Design of Magnitude Comparator using Modified Positive Feedback Adiabatic Logic Technique

This part provides the design of a modified PFAL based magnitude comparator circuit. It uses an additional DC voltage source. Between the source and ground terminals, a PFAL cross-coupled inverter is connected. During the evaluation phase, the logic is evaluated according to the input vectors during the hold stage.

The MPFAL comparator using a stage shifting technique with a DC voltage (Vdc) source and power clocks (Vpc) is depicted in Figure 4. The circuit is simulated at 0.1V. MPFAL achieves low power operation due to low Vdc as connected in series. When Vdc is increased, the lower limit of the output waveform tends to reduce.

The performance metrics such as power dissipation of 4.12μw, delay of 66.1ns, PDP of 0.27pj, the rise time of 6.707 ns, and the fall time of 49.59 ns at 1.8V are obtained for the proposed MFAL based 1-bit magnitude comparator circuit. The parameters justify the improved performance of the proposed circuit.

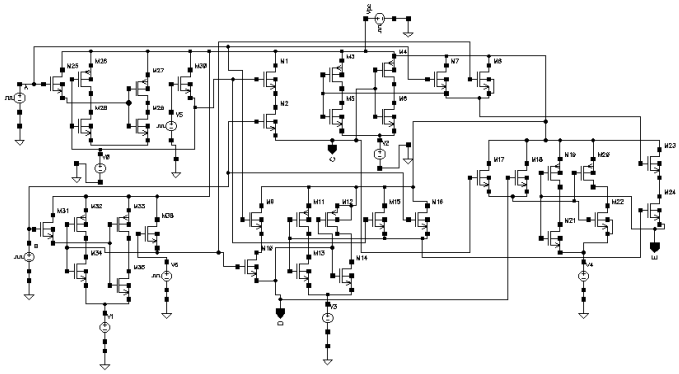

Figure 4. MPFAL based comparator

3.4 Design of Magnitude Comparator using Direct Current Diode Based Positive Feedback Adiabatic Logic Technique

The design of 1-bit magnitude comparator using direct current diode based PFAL technique is presented in this section. Figure 5 depicts the proposed logic generalized circuit diagram. Similar to PFAL logic, the transmission gates are formed by connecting the functional blocks of NMOS logic in parallel with the PMOS transistors of the latch. The distinction was its pull-down blocks through the NMOS diode as well as DC voltage sources connecting between the NMOS transistors and ground. The principle behind the usage of the diode at the base of NMOS tree is that it assists to regulate the discharging direction by reducing the rates of discharge of logic circuit internal nodes. A positive DC voltage of 0.1V is attached to the diode due to the benefits of the level shifting technique. The leakage current of the output transistor and the gate to source voltage are reduced due to level shifting.

The simulation results shows that the parameters such as energy dissipation of 1.25 μW, delay of 65.91 ns, power delay product of 0.082 pJ, rise time of 0.006 ns, and fall time of 19.54 ns at 1.8V are obtained for the proposed DC-DB PFAL 1-bit magnitude comparator circuit, which shows its better performance as compared to the previously executed circuits.

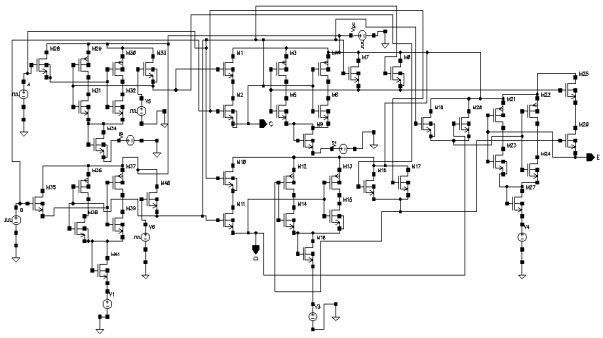

Figure 5. DC-DB PFAL based comparator

4 Results and Discussion

The simulations are performed and the results are obtained at 180nm technology node using cadence virtuoso tool. All the proposed ECRL, PFAL, MPFAL and DC-DB PFAL 1-bit magnitudes comparator architectures are designed and simulated at 1.8V supply at different frequencies. The analysis

is carried out for various parameters and the results are compared.

Table 1 compares the power dissipation analysis of various 1-bit magnitude comparators at different frequencies *viz* 6MHz, 100MHz, and 500Hz. At these frequencies, the PD of the DC-DB PFAL 1-bit magnitude comparator is found lower than that of other adiabatic approaches.

The proposed DC-DB PFAL based 1-bit magnitude comparator has shown a power dissipation improvement of 69%, 94% and 90% as compared to the other proposed designs of MPFAL, PFAL and ECRL circuits respectively at 6MHz.

At 100 MHz, power dissipation of proposed 1-bit magnitude comparator is improved by 86 %, 91%, and 83 % when compared to ECRL, PFAL, and Modified PFAL circuits respectively. In DC-DB PFAL, it is observed that as the frequency is increased, the performance is degrading. Yet, it is distinguished that the PD of the proposed design is much improved than other adiabatic approaches.

Table 1. Comparison of PD (power dissipation) for the proposed 1-bit comparator using different adiabatic approaches

Si. No.	Comparator	PD (µw) At 500 MHZ	PD (µw) At 100 MHZ	PD (µw) At 6 MHZ
1	ECRL	77.57	158.2	13.19
2	PFAL	114.1	239.9	22.54
3	MPFAL	110.1	125.2	4.12
4	DC-DB PFAL	32.76	21.81	1.25

Another important parameter is the propagation delay. The delay of the proposed DC-DB PFAL based 1-bit magnitude comparator has shown an improvement of 3%, 2%, and 1% at 6MHz as compared to other designs. Further, an improvement of 7% and 2% is observed at 100MHz compared to designs using PFAL and Modified PFAL techniques. Table 2 demonstrates the performance of the proposed design is degrading as the frequency increases.

Table 2. Delay comparison for the proposed 1-bit comparator using different adiabatic approaches

Si. No.	Comparator	Delay (ns) At 500 MHZ	Delay (ns) At 100 MHZ	Delay (ns) At 6 MHZ
1	ECRL	26.49	6	67.87
2	PFAL	28.58	6.45	67.3
3	MPFAL	26.27	6.12	66.1
4	DC-DB PFAL	29.03	6	65.91

Moreover, the power delay product (PDP) for DC-DB PFAL based 1-bit magnitude comparator with respect to Modified PFAL, PFAL and ECRL based comparator, gives an improvement of 69 %, 94% and 90% at 6MHz and 83%, 91% and 86% at 100MHz respectively. Thus, it is found that the proposed design based on direct current diode based positive feedback adiabatic logic shows an improved performance for power delay product at different frequencies as shown in Table 3.

Table 3. PDP (power delay product) comparison for the proposed 1-bit comparator using various adiabatic approaches

Si. No.	Comparator	PDP (pJ) At 500 MHZ	PDP (pJ) At 100 MHZ	PDP (pJ) At 6 MHZ
1	ECRL	2.054	0.947	0.895
2	PFAL	3.260	1.549	1.516
3	MPFAL	2.892	0.766	0.272
4	DC-DB PFAL	0.951	0.130	0.082

Similarly, the other parameters investigated are RT and FT of the proposed 1-bit magnitude comparator. Table 4 and Table 5 demonstrate the RT and FT for various adiabatic designs at different frequencies. According to the simulation results, it is found that the DC-DB PFAL based 1-bit magnitude comparator design have superior performance compared to the other techniques.

Table 4. Rise Time (RT) comparison for the proposed 1-bit comparator using different adiabatic approaches

Si. No.	Comparator	RT (ns) At 500 MHz	RT (ns) At 100 MHz	RT (ns) At 6 MHz
1	ECRL	1.35	0.990	0.974
2	PFAL	0.642	4.24	9.024
3	MPFAL	0.749	0.993	67.07
4	DC-DB PFAL	0.625	1.003	0.006

Table 5. Fall Time (FT) comparison for the proposed 1-bit comparator using different adiabatic approaches

Si. No.	Comparator	FT (ns) At 500 MHz	FT (ns) At 100 MHz	FT (ns) At 6 MHz
1	ECRL	7.76	11	13.52
2	PFAL	5.77	4.24	510.6
3	MPFAL	7.76	4.24	495.9
4	DC-DB PFAL	7.20	7.20	195.4

Finally, transistor count using DC-DB PFAL, Modified PFAL, ECRL and PFAL circuits based 1-bit magnitude comparator are obtained. As illustrated in Figure 6, in comparison to other methods, the proposed DC-DB PFAL circuit requires an additional transistor to implement.

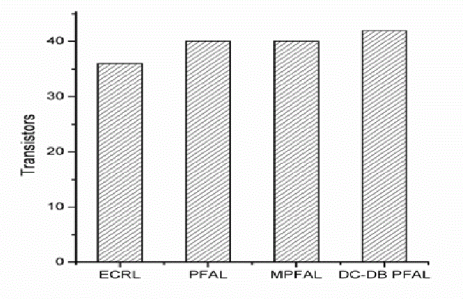

Figure 6. Comparison of transistor count for 1- bit comparator

Further, the output waveform of the 1-bit magnitude comparator based on DC-DB PFAL circuit is represented in Figure 7, the corresponding outputs (C), (D) and (E) waveforms are obtained to inputs (A), (B) and power clock (Vpc) combinations.

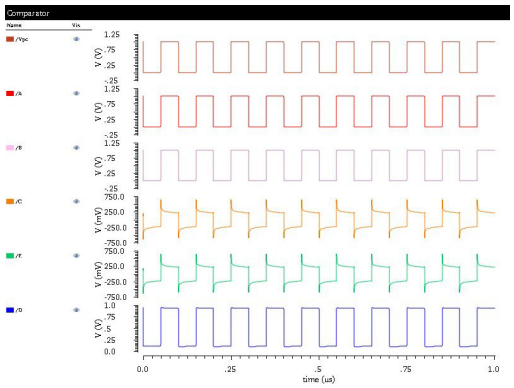

Figure 7. Output waveform of the proposed circuit

Table 6 shows a comparative analysis of the all proposed designs with the adiabatic as well as non adiabatic circuits as evidenced by research survey. It is observed that the proposed 1-bit comparator based on DC-DB PFAL shows the superior performance in terms of energy dissipation and PDP. Furthermore, it is analyzed that 1-bit comparator circuit based on direct current diode based PFAL technique requires more transistors compared to the other designs. However, it is observed that proposed 1-bit comparator design using direct current diode based PFAL technique require lesser number of transistors compared with the designs in the existing literature.

Table 6. Comparative analysis of different types of comparators available in literature with the proposed designs

Types of comparator	Freq.	T	PD (µW)	D (ns)	PDP (pJ)	Ref.	Technology (nm)
1-bit comparator (adiabatic)	8 MHz	-	4.202	-	-	[18]	90
2-bit comparator ECRL (adiabatic)	-	110	23.73	3505000	8313650	[15]	90
2-bit comparator PFAL (adiabatic)	-	92	1.634	4613900	7539112.6	[15]	90
4-bit comparator CMOS (non- adiabatic)	167 MHz	116	4400	-	-	[14]	180
4-bit comparator ECRL (adiabatic)	167 MHz	124	2000	-	-	[14]	180
4-bit comparator PFAL (adiabatic)	167 MHz	124	2000	-	-	[14]	180
64-bit comparator using CMOS technology (non-adiabatic)	-	-	1720	130.69	22700	[26]	180
4-bit comparator (adiabatic)	-	116	113.11	17.715	1.987	[27]	-
Single tail dynamic comparator	800 MHz	9	15.54	13.8	214.45	[11]	180
Double tail dynamic comparator	1.6 GHz	12	29.21	500	14605	[11]	180
Double tail comparator with enhanced latch regeneration	2.2 GHz	16	28.23	420	11856	[11]	180
Proposed dynamic comparator	2.24 GHz	20	24.64	426	10496	[11]	180
Proposed 1-bit ECRL comparator	6 MHz	36	13.19	67.87	0.895	-	180
Proposed 1-bit PFAL comparator	6 MHz	38	22.54	67.3	1.516	-	180
Proposed 1-bit MPFAL comparator	6 MHz	38	4.12	66.1	0.272	-	180
Proposed 1-bit DC-DB PFAL comparator	6 MHz	40	1.25	65.91	0.082	-	180

Where, T, D, PD and PDP are Transistor Count, Delay, Power dissipation and power delay product respectively.

5 Conclusion

In this paper, the architectures of a 1-bit magnitude comparator employing direct current diode based PFAL and MPFAL, PFAL and ECRL techniques are designed and simulated at 180nm technology node. The analysis is carried out for the performance measurements of power consumption, delay, rise time, falls time, transistor count and PDP. The proposed designs are compared together along with the non adiabatic and adiabatic designs reported in the literature.

Moreover, the proposed design using DC-DB PFAL excels with a 69 % of improvement in power dissipation over the other proposed MPFAL based design at 6MHZ. This shows that the proposed design based on DC-DB PFAL outperforms over the other adiabatic and non adiabatic techniques and hence can contribute significantly towards low power. Number of bits of the comparator can be increased; keeping in view the transistors count also for future investigations and IOT applications.

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